



## SSC8415GS6

### P-Channel Enhancement Mode MOSFET

#### ➤ Features

$V_{DS}$	$V_{GS}$	$R_{DS(ON)}$ Typ.	$I_D$
-20V	$\pm 12V$	35m $\Omega$ @-4V5	-4A
		44m $\Omega$ @-2V5	

#### ➤ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

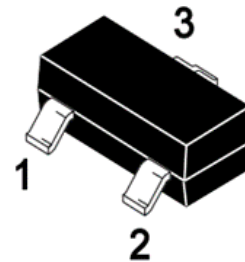
#### ➤ Applications

- Load Switch
- Portable Devices
- DCDC Conversion

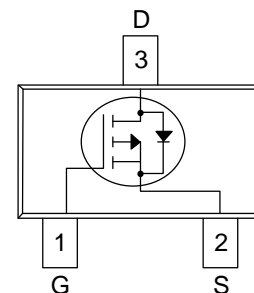
#### ➤ Ordering Information

Device	Package	Shipping
SSC8415GS6	SOT-23	3000/Reel

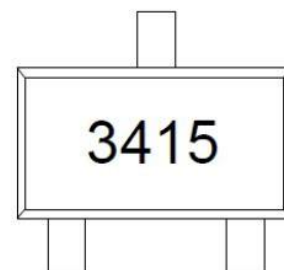
#### ➤ Pin configuration



**SOT-23**



**Pin Configuration (Top View)**



**Marking**



➤ **Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	-20	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current <sup>a</sup>	-4	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	-22	A
$P_D$	Power Dissipation <sup>c</sup>	0.9	W
$P_{DSM}$	Power Dissipation <sup>a</sup>	0.55	W
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>	140	$^{\circ}\text{C/W}$

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper, in a still air environment with  $T_A=25^{\circ}\text{C}$ . The value in any given application depends on the user is specific board design. The power dissipation is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

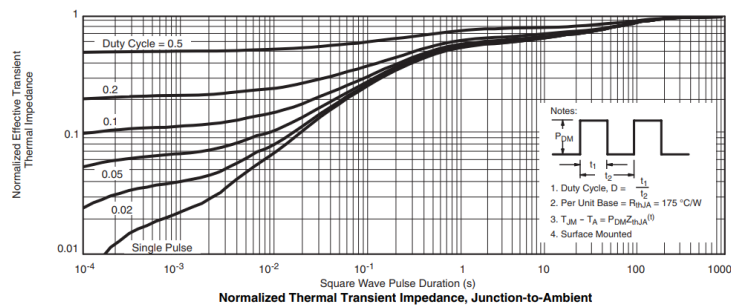
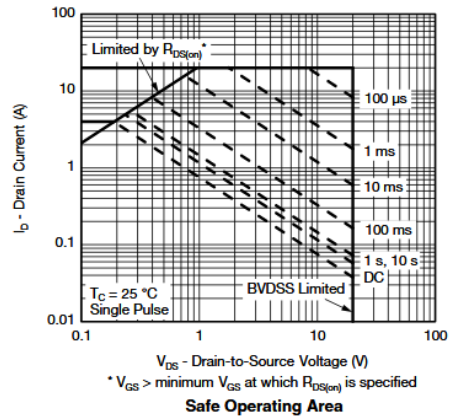
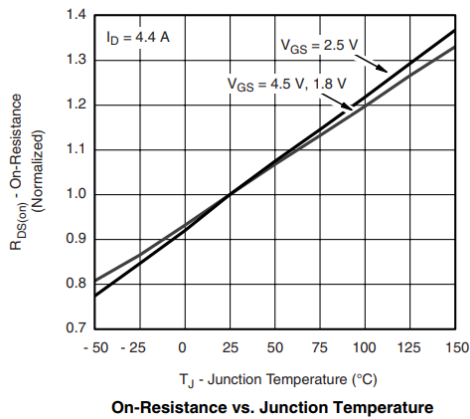
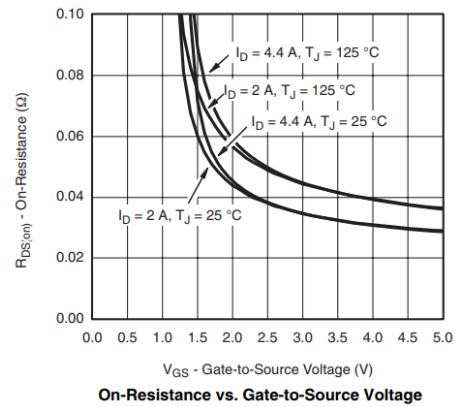
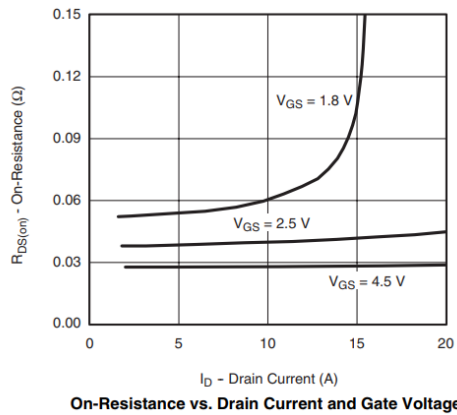
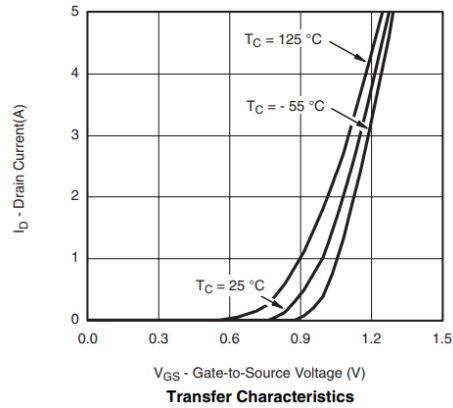
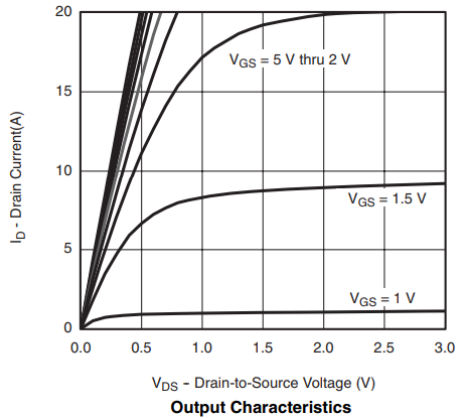


➤ **Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)**

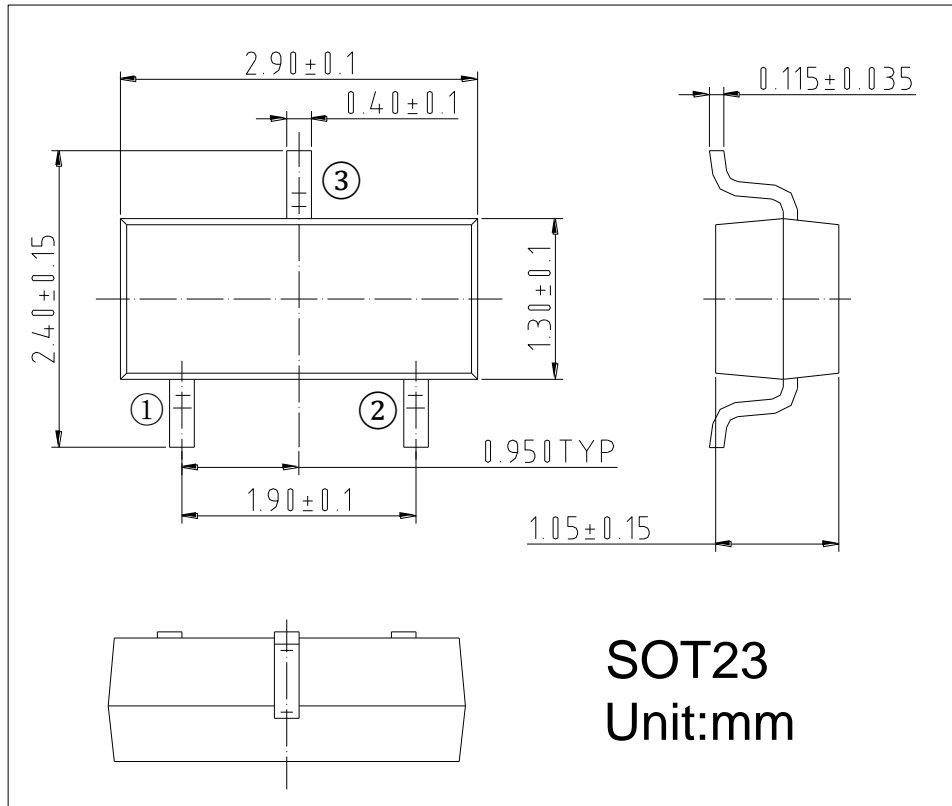
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-10uA	-20			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-0.4	-0.6	-0.9	V
Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3.5A		35	40	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-3A		44	65	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V			-1	μA
Gate-Source Leak Current	I <sub>GSS</sub>	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V			±100	nA
Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1.6A	-0.5	-0.75	-1.2	V
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V, f = 1MHz		869		pF
Output Capacitance	C <sub>OSS</sub>			265		
Reverse Transfer Capacitance	C <sub>RSS</sub>			258		
Turn-on Delay Time	T <sub>D(ON)</sub>	V <sub>DS</sub> =-10V,  I <sub>D</sub> =-1.0A, R <sub>L</sub> =6Ω,  V <sub>GS</sub> =-4.5V, R <sub>G</sub> =6Ω,		12		ns
Rise Time	T <sub>r</sub>			8.9		
Turn-off Delay Time	T <sub>D(OFF)</sub>			45		
Fall Time	T <sub>f</sub>			15		
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =-4.5V,  I <sub>D</sub> =-5A		12		nC
Gate to Source Charge	Q <sub>GS</sub>			2.1		
Gate to Drain Charge	Q <sub>GD</sub>			2.4		



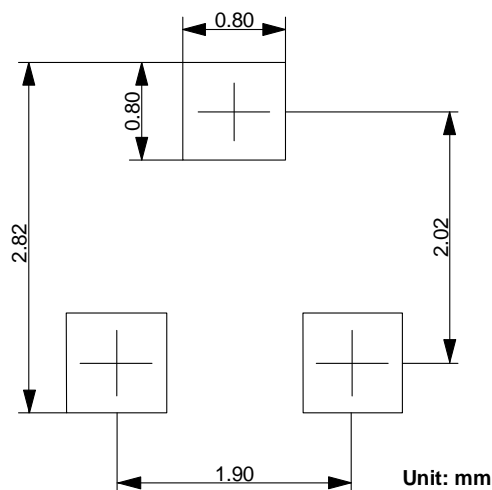
## ➤ Typical Performance Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)



## ➤ Package Information



## ➤ Recommended Pad outline





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